Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in this application.

1. (Cancelled).

2. (Previously Presented) A method for demodulating a frequency-modulated signal, comprising:

generating a first signal by fixing the modulated signal amplitude at a predetermined level;

generating a second signal by delaying the first signal;

generating an output signal by determining the cross product of the first signal and the second signal, wherein the second signal is delayed by a length of time such that the phase angle between the first and second signals is less than .2 pi, whereby the step of determining the cross product can be performed using a small-angle approximation, whereby the output signal is representative of the demodulated signal.

3. (Cancelled).

4. (Currently Amended) A method for demodulating a frequency-modulated signal, comprising:

generating a first digital signal by fixing the modulated signal amplitude at a predetermined level, wherein fixing the modulated signal amplitude is performed by applying the signal to a limiting amplifier;

generating a second digital signal by delaying the first signal;

generating an output signal by determining the cross product of the first digital signal and the second digital signal, wherein generating the first signal comprises the following substeps:

applying the signal to a limiting amplifier; and

digitizing the output of the limiting amplifier;

whereby subsequent steps are performed in the digital signal domain, whereby the output signal is representative of the demodulated signal.

5. (Original) The method of claim 4, in which the substep of digitizing the output of the limiting amplifier is performed by applying the output of the limiting amplifier to a flip-flop, whereby the flip-flop acts as a 1-bit analog-to-digital converter.

6. (Cancelled).

7. (Previously Presented) A method for demodulating a frequency-modulated signal, comprising:

generating a first signal by fixing the modulated signal amplitude at a predetermined level;

generating a second signal by delaying the first signal;

generating an output signal by determining the cross product of the first signal and the second signal,

squaring up the demodulated output signal by applying the output signal to a data slicer, wherein squaring up the demodulated output signal comprises the following substeps:

generating a reference level signal by lowpass filtering the cross-product output;

applying the output signal and the reference level signal to the inputs of a comparator; whereby the comparator output consists of the squared up demodulated signal, whereby the output signal is representative of the demodulated signal.

8. (Previously Presented) The method of claim 7, further comprising the step of applying the data slicer output to a matched filter to reduce the likelihood of errors in the demodulated signal.

9. (Previously Presented) The method of claim 8, in which the number of taps in the matched filter is equal to the ratio between the data rate of the data slicer output and the bit rate of the demodulated signal.

10. (Cancelled).

11. (Cancelled).

12. (Previously Presented) A method for demodulating a frequency modulated signal, comprising:

amplifying the modulated signal using a limiting amplifier;

digitizing the limited signal using an analog-to-digital converter;

applying the digitized limited signal to a quadrature demodulator to create a first I signal and a first Q signal;

creating a second I signal by delaying the first I signal;

creating a second Q signal by delaying the first Q signal;

generating a first product by multiplying the first I signal by the second Q signal;

generating a second product by multiplying the first Q signal the second I signal; and

subtracting the second product from the first product to generate the demodulated signal, wherein the second I signal and the second Q signal are each delayed by one sample.

13. (Cancelled).

14. (Previously Presented) A method for demodulating a frequency modulated signal, comprising:

amplifying the modulated signal using a limiting amplifier;

digitizing the limited signal using an analog-to-digital converter;

applying the digitized limited signal to a quadrature demodulator to create a first I signal and a first Q signal;

creating a second I signal by delaying the first I signal;

creating a second Q signal by delaying the first Q signal;

generating a first product by multiplying the first I signal by the second Q signal;

generating a second product by multiplying the first Q signal the second I signal;

subtracting the second product from the first product to generate the demodulated signal;

squaring up the demodulated signal by applying the demodulated signal to a data slicer, wherein squaring up the demodulated signal is comprised of the following substeps:

generating a reference level signal by lowpass filtering the demodulated signal; comparing the demodulated signal with the reference level signal to generate a squared up output signal.

15. (Previously Presented) The method of claim 14, further comprising the step of applying the data slicer output to a matched filter to reduce the likelihood of errors in the apparatus output.

16. (Original) The method of claim 15, in which the number of taps in the matched filter is equal to the ratio between the data rate of the data slicer output and the bit rate of the demodulated signal.

17. (Previously Presented) An apparatus for demodulating a frequency modulated signal, the apparatus comprising:

a limiting amplifier, which amplifier's input receives the frequency modulated signal;

an analog-to-digital converter, which converter operationally receives the limiting amplifier output signal and generates a digitized frequency modulated signal;

a cross-product multiplier which receives the digitized frequency modulated signal and outputs the cross-product of the digitized frequency modulated signal with a delayed copy of the digitized frequency modulated signal to generate a demodulated output signal; and

a data slicer with input operably connected to the cross-product multiplier output wherein the data slicer is comprised of:

a lowpass filter, which filter receives the data slicer input;

a comparator with inputs of the data slicer input, and the lowpass filter output, whereby the comparator outputs the squared up demodulated signal.

18. (Original) The apparatus of claim 17, in which the analog-to-digital converter is a flip-flop generating a 1-bit digital output.

19. (Previously Presented) The apparatus of claim 17, in which the cross-product multiplier is comprised of:

a quadrature demodulator with an input connected to the analog-to-digital converter output, which quadrature demodulator generates a baseband I output and a baseband Q output;

a first delay element, which element receives the I output of the quadrature demodulator;

a second delay element, which element receives the Q output of the quadrature demodulator;

a first multiplier, which multiplier has as its inputs the I output of the quadrature demodulator and the output of the second delay element;

a second multiplier, which multiplier has as its inputs the Q output of the quadrature demodulator and the output of the first delay element;

an inverter which receives the output of the second multiplier;

an adder, which adder has as its inputs the output of the first multiplier and the output of the inverter;

whereby the adder output is the demodulated signal.

20. (Cancelled).

21. (Cancelled).

22. (Currently Amended) The apparatus of claim 19 ~~20~~, the apparatus further including a matched filter with input operably connected to the data slicer output, which matched filter provides for correction of errors in the data slicer output.